13.9 A 10Gb/s Burst-Mode Adaptive Gain Select Limiting Amplifier in 0.13μm CMOS

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Optical packet communication is one of the best candidates for flexible large-capacity low-cost communication. Packet-based systems require burst-mode receivers that amplify input data and extract a synchronous clock instantaneously for each asynchronous packet. Previous integrated burst-mode receiver ICs operate at up to 1.25Gb/s [1-3], and a 10Gb/s burst-mode monolithic clock and data recovery (CDR) IC was reported last year [4]. This paper describes a 10Gb/s burst-mode, wide-dynamic-range limiting amplifier without reset signal. It can instantaneously amplify input data within a settling time of 0.8ns (8 bits) over a dynamic range of 28dB. The dynamic range is five times wider than that of the previous work [4].

Limiting amplifier circuits used for burst-mode receivers can be divided into two types. One is the average-level detecting type [1-3], which generates the reference level from the high and low levels of the input burst signal for amplifying the signal at a current switch. Fixing the reference level at one stable level takes time, so such circuits require a long settling time of 20ns. On the other hand, the data-edge detecting type [4] can, in theory, amplify input data from the first bit for each packet without a preamble (Fig. 13.9.1). In addition, this type can operate without a reset signal and enables the use of an ac-coupled input. The data-edge detecting type consists of a delay line, differential amplifiers, and a hysteretic comparator. The delay line and the amplifiers detect input data edges and generate narrow edge pulses. The widths of the pulses are the delay times of the delay line. The comparator recovers the original NRZ data. A problem with this type of amplifier is that noise on the input signal is also amplified with the signal and works as the edge pulse. In general, as the input signal-swing increases, noise becomes larger. When the input signal-swing is several hundred millivolts, the noise amplitude is probably over 10mV. If the amplifier is designed to have a gain of 26dB, it amplifies a 10mV noise pulse to a pulse of 200mV. Such a noise pulse easily triggers the output of the hysteretic comparator, thereby causing a bit error. As a result, the previous work using data-edge detection has a narrow dynamic range of 14dB. The limiting amplifier presented here improves the dynamic range by adaptive gain selection.

Figure 13.9.2 shows a circuit diagram for the data-edge detecting amplifier with adaptive gain selection. The amplifier has a delay line, five amplifying paths, and five hysteretic comparators. Each path amplifies an edge pulse with a different gain. The five comparators operate to recover the original NRZ data in parallel. The adaptive gain selection circuit is composed of the four signal detectors (DET) and a logic circuit that sends a 4b selection signal to the selector (SEL). The selection signal chooses the input with the lowest bit-error rate. To find the input with the lowest bit-error rate, the adaptive gain selection circuit determines the amplifying path with the proper gain for the current input signal swing. Here the proper gain path means the path having the second lowest gain among the paths that can recover input data at the hysteretic comparators; this path is chosen because the lowest gain increases the possibility of missing the data edge and higher gain causes surplus amplification of input noise as mentioned above.

Figure 13.9.3 shows the DET, which detects the existence of data transitions. When the peak hold circuit receives data transitions, the circuit pulls both nodes $n1$ and $n2$ high and charges capacitors $C1$ and $C2$ through transistors $M1$ and $M2$ within as little as a few bit times. When the peak-hold circuit receives consecutive low data, the circuit pulls node $n2$ low by discharging capacitor $C2$ through resister $R2$, which can take as long as 150 bit times. This duration is two times longer than 72 consecutive identical digits. The hysteretic comparators in the DET prevent the output from chattering. The four DET outputs (B2, C2, D2 and E2) show a bit pattern dependent on the input signal swing, as summarized in the truth table in Fig. 13.9.2. The logic in the adaptive gain selection circuit outputs the 4b selection signal to the SEL block in order to select one of the paths (A1, B1, C1 or D1) as specified in the table. The time required for the selection is the sum of the latency of the DET, logic, and the SEL blocks. This time is around an 8-bit cycle, so the settling time of the limiting amplifier is under 1ns at 10Gb/s.

The amplifier IC was fabricated in a 0.13μm CMOS process. Figure 13.9.4 shows a micrograph of the chip. The chip size is $1.6\times1.7mm^2$. The evaluation was done on a bare die with RF probes. Figure 13.9.5 shows the input and output waveforms of the limiting amplifier IC. The input burst signal contains an 8-bit preamble, PN7 bit streams, and 30 consecutive low bits for checking the settling time and tolerance for consecutive identical bits. An error-free ($< 10^{-12}$) output with 400mV swing was confirmed at 10Gb/s with an input signal-swing between 40 and 1000mV. The measured settling time was as fast as 0.8ns (8 bit times) over the input signal-swing range. The IC consumes 500mW from a 2.5V power supply with an output buffer included.

Figure 13.9.6 compares the measured dynamic range of this amplifier and the previous one [4]. Error-free ($< 10^{-12}$) operation is obtained for input signal swings from 40 to 1000mV, i.e., the dynamic range of 28dB is achieved. In comparison with the 14dB DR of the previous circuit, the dynamic range is improved five-fold. Figure 13.9.7 summaries the performance of the amplifier IC.

Acknowledgement:
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References:
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[4] M. Nogawa et al., "A 10Gb/s Burst-Mode CDR IC in 0.13μm CMOS," *IEEE ISSCC Dig. Tech. Papers*, pp. 228-229, Feb., 2005.

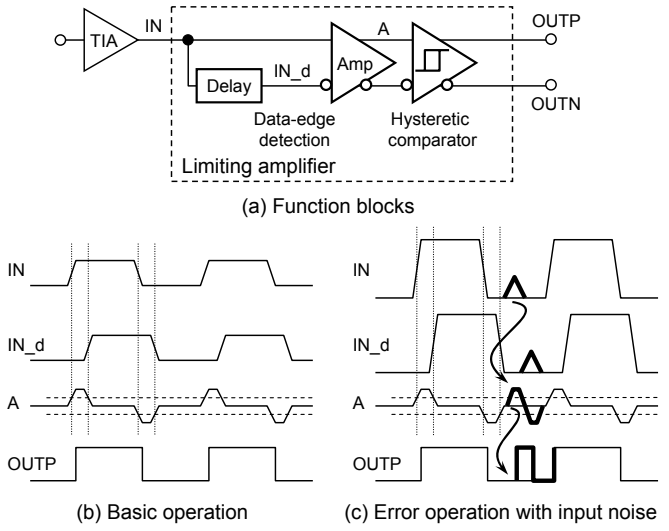

Figure 13.9.1: Burst-mode limiting amplifier with data-edge detection.

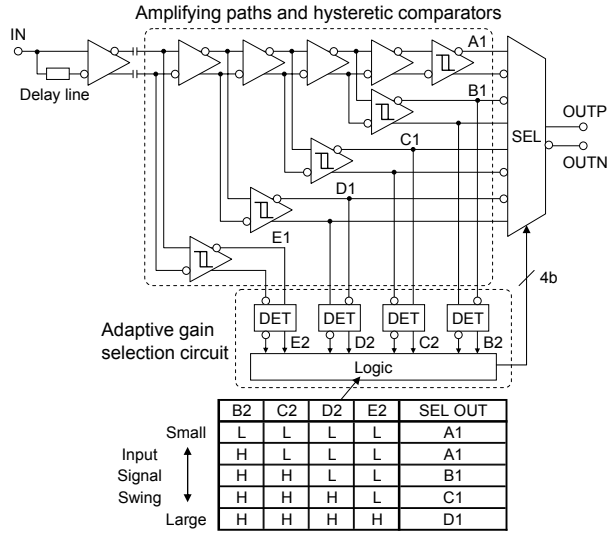

Figure 13.9.2: Data-edge detection limiting amplifier with adaptive gain selection.

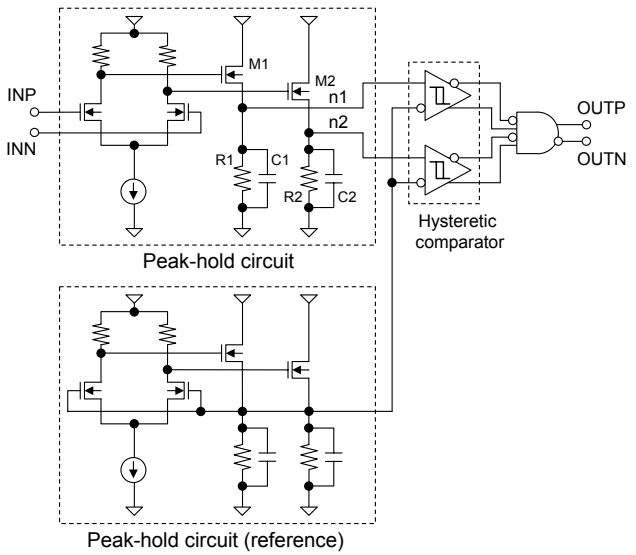

Figure 13.9.3: Signal detector (DET).

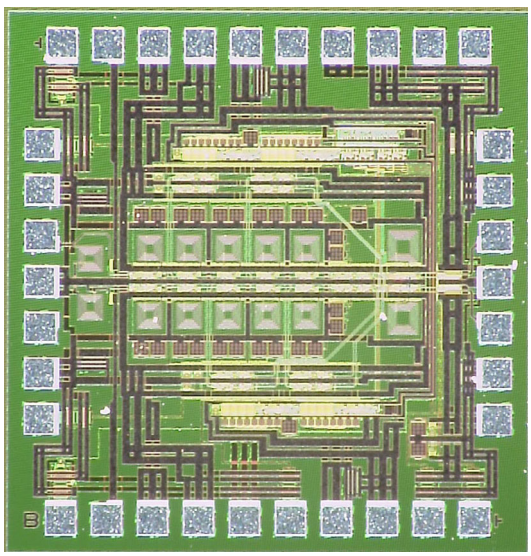

Figure 13.9.4: Chip micrograph.

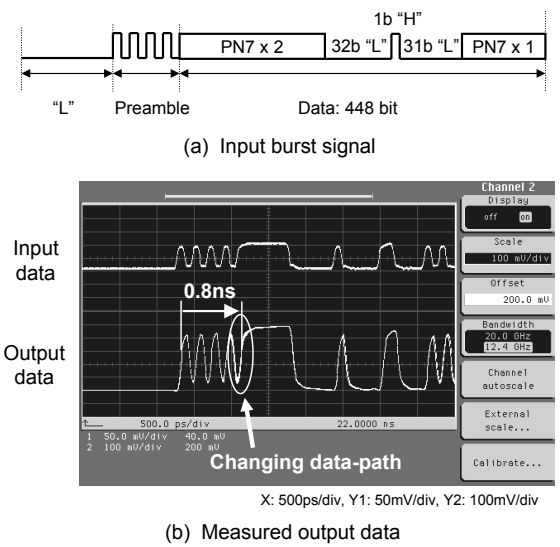

Figure 13.9.5: Bust-mode amplification with adaptive gain selection.

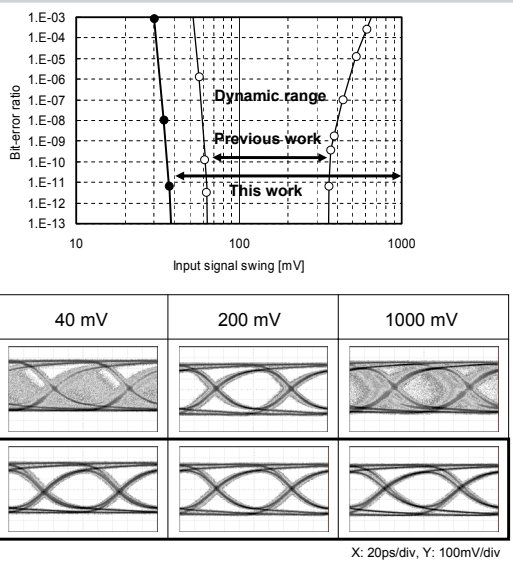

Figure 13.9.6: Measured dynamic range and eye patterns for 2^{31}-1 PRBS.

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Process technology	0.13μm CMOS	f_T=70GHz
Data rate	10Gb/s	for burst and PRBS data
Input sensitivity	40mV	Dynamic range > 28dB
Input overload	> 1000mV	
Settling time	< 1ns	
External reset	No need	
Output swing	800mV_{pp}	Differential peak to peak
Supply voltage	2.5V	
Die size	1.6 x 1.7mm^2	

Figure 13.9.7: Performance summary.

